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Substitute for form 1449A/PTO				Application Number	09/737,245
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Filing Date	12/13/00
				First Named Inventor	Steven Teig
				Group Art Unit	2825
				Examiner Name	Thuan Do
Sheet	1	of	3	Attorney Docket Number	SPLX.P0012

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U.S. PATENTS RELATED TO THE PRESENT APPLICATIONS						
Examiner Initials	Cite No. ¹	U.S. Patent Document Number	Kind Code ² (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication MM-DD-YYYY	Relation to Present Application
TD	1.	6,516,455	B1	Teig, et al.	02-10-02	CIP of the parent application of the present application

U.S. PATENT DOCUMENTS						
Examiner Initials	Cite No. ¹	U.S. Patent Document Number	Kind Code ² (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
TD	2.	2001/0003843	A1	Scepanovic et al.	06-14-01	
	3.	4,615,011		Linsker	09-30-86	
	4.	5,097,422		Corbin, II et al.	03-17-92	
	5.	5,532,934		Rostoker	07-12-96	
	6.	5,566,078		Ding et al.	10-15-96	
	7.	5,578,840		Scepanovic et al.	11-26-96	
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	9.	5,636,125		Rostoker et al.	06-03-97	
	10.	5,650,653		Rostoker et al.	07-22-97	
	11.	5,742,086		Rostoker et al.	04-21-98	
	12.	5,757,656		Hershberger et al.	05-26-98	
	13.	5,777,360		Rostoker et al.	07-07-98	
	14.	5,811,863		Rostoker et al.	09-22-98	
	15.	5,822,214		Rostoker et al.	10-13-98	
	16.	5,859,449		Kobayashi et al.	01-12-99	
	17.	5,898,597		Scepanovic et al.	04-27-99	
	18.	5,914,887		Scepanovic et al.	06-22-99	
	19.	6,035,108		Kikuchi	03-07-00	
TD	20.	6,058,254		Scepanovic et al.	05-02-00	

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				Examiner Name		Thuan Do FEB 02 2004	
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U.S. PATENT DOCUMENTS						
TD	21.	6,068,662		Scepanovic et al.	05-30-00	
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TD	40.	JP	64-15947		Ouchi	01-19-89		

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TD	42.	C. Chiang, et al., Wirability of Knock-Knee Layouts with 45° Wires, IEEE Transactions on Circuits and Systems, Vol. 38, Issue 6, pp 613-624, June 1991.		
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TD	45.	J. Vicente, RSR: A New Rectilinear Steiner Minimum Tree Approximation for FPGA Placement and Global Routing, Proceedings of the 24 th Euro Micro Conference, pp 192-195, August 1998.		
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TD	49.	M. Igarashi et al., A Diagonal-Interconnect Architecture and Its Application to RISC Core Design, 2002 IEEE Solid-State Circuits Conference, pp 210-460, February 2002.		
TD	50.	P. Dood, et al. A Two-Dimensional Topological Compactor with Octagonal Geometry, 28 th ACM/IEEE Design Automation Conference, pp 727-731, July 1991.		
TD	51.	P. Parikh, et al., Congestion Driven Quadratic Placement, Proceedings of Design Automation Conference, 1998, pp 275-278.		
TD	52.	R. Putatunda et al., VITAL: Fully Automatic Placement Strategies for Very Large Semicustom Designs, Proceedings of the International Conference on Computer Design: VLSI in Computers and Processors, pp 434-439 October 1988.		
TD	53.	Y. Sekiyama et al., Timing-Oriented Routers for PCB Layout Design of High-Performance Computers, International Conference on Computer Aided Design, pp 332-335, November 1991.		

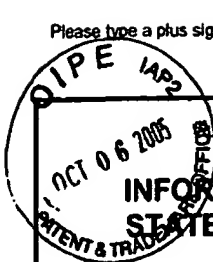
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		Office ³	Number ⁴	Kind Code (if known) ⁵				
TD	1.	JP	411296560	A	10-29-1999	Matsumoto et al.	with English translation of Abstract;	
TD	2.	JP	2000-82743	A	03-21-2000	Igarashi et al.	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.	✓
TD	3.	JP	H03-173471	A	07-26-1991	Tawada et al.	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.	✓
TD	4.	JP	H05-243379	A	09-21-1993	Masako Kubota	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.	✓
TD	5.	JP	H05-102305	A	04-23-1993	Akihiro Sato	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.	✓
TD	6.	JP	H07-086407	A	03-31-1995	Shinpei Miura	with Japanese Patent Office's English translation of Abstract; and with English translation of the	✓

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FOREIGN PATENT DOCUMENTS							
							application.
TD	7.	JP	H09-162279	A	06-20-1997	Masaaki Yoshida	with Japanese Patent Office's English translation of Abstract; and with English translation of the application.
TD	8.	JP	02-262354		10-25-1990	Kuribayashi, Mototaka	✓

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Sheet	5	of	5	Attorney Docket Number	SPLX.P0012

NON PATENT LITERATURE DOCUMENTS			
TD	35.	Takashima, Y. et al, Routability of FPGAs with Extremal Switch-Block Structures, IEICE Trans. Fundamentals, vol. E81-A, No. 5, May 1998, pp. 850-856.	
TD	36.	Thakur, S. et al., Algorithms for a Switch Module Routing Problem, 1994, pp. 265-270.	
TD	37.	Theune, D. et al., HERO: Hierarchical EMC-constrained routing, 11/1992, IEEE pp 468-472.	
TD	38.	Tseng, H., Timing and Crosstalk Driven Area Routing, pp. 378-381.	
TD	39.	Wang, D., Novel Routing Schemes for IC Layout, Part I: Two-Layer Channel Routing, 28 th ACM/IEEE Automation Conference, 1991, pp. 49-53.	
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TD	42.	Zhang, C.X. et al., Floorplan Design Using a Hierarchical Neural Learning Algorithm, IEEE, 6/1991. pp. 2060-2063.	
TD	43.	Zhou, H. et al., An Optimal Algorithm for River Routing with Crosstalk Constraints, 1996.	
TD	44.	Zhou, H. et al., Global Routing with Crosstalk Constraints, Department of Computer Sciences, University of Texas, 1998, pp. 374-377.	
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TD	46.	Cong J. et al., DUNE - Amultilayer Gridless Routing System, May 2001, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, vol 20, iss. 5, pp.633-647	

Examiner Signature	<i>Thuan V. Do</i>	Date Considered	2-17-06
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